FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several she ts if nec ssary)	ATTY. DOCKET NO. 200313631-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Stephen R. Van Doren, t al.		
	FILING DATE herew ith	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	2001/0034815	10/25/2001	Dungan, et al.	
	1B	2002/0009095	01/24/2002	Van Doren, et al.	
	1C	2002/0073071	06/13/2002	Pong, et al.	
	1D	2003/0018739	01/23/2003	Cypher, et al.	
	1E	2003/0140200	07/24/2003	Jamil, et al.	
	1F	2003/0145136	07/31/2003	Tierney, et al.	
	1G	2003/0195939	10/16/2003	Edirisooriya, et al.	
	1H	2003/0200397	10/23/2003	McAllister, et al.	
	1I	5,802,577	09/01/1998	Bhat,et al.	
	1J	5,829,040	10/27/1998	Son	
	1K	5,875,467	02/23/1999	Merchant	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	RAJEEV, JOSHI, et al., "Checking Cache-Coherence Protocols with TLA+", Kluwer Academic Publishers, 2003, pp. 1-8
	1R	MARTIN, MILO M.K., et al., "Token Coherence: Decoupling Performance and Correctness", ISCA-30, pp. 1-12, June 9-11, 2003
	1S	ACACIO, MANUEL E., et al., "Owner Prediction for Accelerating Cache-to-Cache Transfer Misses in a cc-NUMA Architecture", IEEE 2002

EXAMINER	DATE CONSIDERED
	6-11-06

FORM PTO-1449	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	200313631-1		
	APPLICANT: St phen R. Van Doren, et al.		
(Use several sheets if necessary)	FILING DATE: herew ith	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	5,875,472	02/23/1999	Bauman, et al.	
	2B	5,958,019	09/28/1999	Hagersten, et al.	
	2C	6,055,605	04/25/2000	Sharma, et al.	
	2D	6,085,263	07/04/2000	Sharma, et al.	
	2E	6,108,737	08/22/2000	Sharma, et al.	
	2F	6,345,342 B1	02/05/2002	Arimilli, et al.	
	2G	6,457,100 B1	09/24/2002	Ignatowski, et al.	
	2H	6,490,661 B1	12/03/2002	Keller, et al.	
	2I	6,631,401 B1	10/07/2003	Keller, et al.	
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	GHARACHORLOO, KOUROSH, et al., "Architecture and Design of AlphaServer GS320", Western Research Laboratory, (Date Unknown)
	2R	GHARACHORLOO, KOUROSH, et al., "Memory Consistency and Event Ordering In Scalable Shared-Memory Multiprocessors", Computer Systems Laboratory, pp. 1-14, (Date Unknown)
	2S	

EXAMINER	DATE CONSIDERED
	6-11-06